An Efficient Technique to Select Logic Nodes for Single Event Transient Pulse-Width Reduction

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35-Word Abstract:
This paper introduces an efficient method to identify logic nodes most likely to generate single-event transients. Selected nodes are hardened by gate resizing. This is integrated with temporal masking to increase fault tolerance.

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Abstract—This paper introduces an efficient method to identify logic nodes most likely to generate single-event transients. Selected nodes are hardened by gate resizing. This is integrated with temporal masking to increase fault tolerance.

Index Terms—Single Event Transient, Soft Error Rate, Temporal Masking, Selective Hardening.

I. INTRODUCTION

As technology scales, the charge required to generate a Single-Event Transient (SET) decreases while the operating frequency of the circuits increases. Due to this combined effect, combinational logic errors are predicted to exceed flip-flop upsets for advanced technologies [1-2]. To prevent the propagation of SETs to the outputs of combinational circuits, techniques to mitigate Single-Event (SE) effects need to be implemented. The most prominent hardening technique, triple-mode redundancy (TMR) requires approximately 3X overhead in terms of area and power. Alternatively, spatial redundancy techniques requiring large number of simulations to harden nodes selectively have been implemented earlier[3-5]. It is however, difficult to determine, a priori, the number of simulation runs required for adequate fault coverage.

This paper describes a cost-effective and fast algorithmic approach to identify the most vulnerable nodes in circuits. The transistors associated with these nodes may be resized to shorten SET pulses. Guard-Gates (also referred to as Muller C elements) may be used to eliminate the shortened SET pulses to achieve desired hardness levels for combinational logic circuits[6, 7]. This combined approach allows the designer to trade-off SET reduction with area, power and speed. The paper is organized as follows: Section II describes the algorithm used to select the most sensitive nodes in the circuit. Section III reports the error rate improvement, and Section IV describes the use of temporal masking to improve the SER.

II. NODE SELECTION ALGORITHM

Whether SETs are latched or not is determined by the effects of electrical, logical, and temporal masking [2, 8].

The probability of latching an SET is typically estimated by simulating transient faults at each node and observing the output change for all input vectors (or at least a large number of inputs) [3-5]. In this work, we use a pattern independent probabilistic technique to determine whether circuit nodes are either in the logic HIGH or LOW state to estimate the node vulnerabilities in an efficient manner.

We define the probability of signals assuming a logic 1(0) value as \( P_{\text{high}}(P_{\text{low}}) \). These probabilities represent the upset vulnerability and logical masking ability of gates. For conciseness, \( P_{\text{high}} \) is used to illustrate the methodology for all calculations included in this summary. The same logic can be extended for \( P_{\text{low}} \) values. \( P_{\text{high}}(P_{\text{low}}) \) represents the percentage of input vectors for which the n-MOSFETs (p-MOSFETs) connected to the node are OFF, making those nodes specifically more vulnerable to n-hits (p-hits) as compared to p-hits (n-hits). Nodes for which \( 0.5 < P_{\text{high}} < 1 \), there is a greater likelihood of those gates being in the logic 1 state. Nodes having higher comparative values of \( P_{\text{high}} \) are therefore indicative of being more probable to producing SETs due to n-hits. As the SET pulse width for n-hits is a direct function of restoring current drive of p-MOSFETs, an increase in p-MOSFET size will decrease the SET pulse-width at these nodes. Conversely nodes having lower comparative values of \( P_{\text{high}} \) are therefore indicative of being more probable to producing SETs due to p-hits. Hardening gates in the circuit corresponding to \( P_{\text{high}} \) values close to 1(0) will bring significant benefit in terms of SET reduction even if p-channel(n-channel) transistors are sized independently of the n-channel(p-channel) transistors. This would result in saving area at the cost of skewing the logic transition times for the gates that are hardened, compared to symmetric gate sizing.

The value of \( P_{\text{high}} \) also provides insight about the ability of gates to logically mask transients from further propagation. In this paper, gates have been selected for resizing based on their \( P_{\text{high}} \) values and logical masking ability. This approach can be integrated with temporal masking achieved by including variable-delay Guard Gates(GG) at the inputs of receiving flip-flops.

The following discussion demonstrates the use of \( P_{\text{high}} \) to identify the most vulnerable gates in the circuit. The calculation of node signal probabilities is described in [9, 10]. The inputs to the system are assumed to be uncorrelated. For uncorrelated inputs, if \( P1 \) and \( P2 \) (representing \( P_{\text{high}} \)) are input signal probabilities to an AND gate, the output signal...
probability is given by \((P1\cdot P2)\). For an OR gate the value is 
\((P1 + P2) - (P1\cdot P2)\). For an inverter, the output signal
probability is \((1 - P)\). To suppress the effects of signal
correlations and re-convergent fan-outs, literals in products
that are repeated are accounted for only once. For example, in
the probability equation of a gate, if the term \(P_i\) is repeated in
a product, it is accounted for only once. \(P_{high} + P_{low} = 1\). Also
the product of probabilities of inverted signals is 0,
i.e., \(P(i)(1-P(i)) = 0\).

For the circuit shown in Fig. 1, the probability \(P_{high}\) for node
D is
\[ P(D) = P(A.B) + P(A.C) - P(A.B)P(A.C) \]  
(1)

![Fig. 1 Representative circuit for which probability and Failure Metric values have been found](image)

But since the inputs are uncorrelated,
\[ P(A.B) = P(A)\cdot P(B) \quad \text{And} \quad P(A.C) = P(A)\cdot P(C) \]

Suppressing term \(P(A)\) in the third term in (1) we get
\[ P(F) = P(A)P(B) + P(A)P(C) - P(A)P(B)P(C). \]  
(2)
\[ P(Z) = P(A,B') + P(D) - P(A,B')P(D). \]  
(3)

Expanding using the rules above, we get
\[ P(Z) = P(A)P(B)' + P(A)P(B) + P(A)P(C) - P(A)P(B)P(C) - P(A)P(B)'P(C) = P(A). \]  
(4)

This satisfies the Boolean equation in which \(Z = A\) on
minimization. The probability values for each node in the
circuit are given in Column 2 of Table1.

Based on the above analysis the signal probabilities have
been calculated for the International Symposium on Circuits
script operating on a Verilog description of the circuits. Inputs
were assumed uncorrelated and were assigned \(P_{high} = 0.5\).
However the designer can use appropriate probabilities for
specific applications for the given circuit. The advantage of
using raw \(P_{high}\) values in the circuit is that they represent the
probability of upsets due to n-hits or p-hits and can be used to
resize n-MOS or p-MOS arrays separately. The nodes in the
circuit having values \(P_{high}\) close to 1, are more vulnerable to n-
hits producing upsets, while those having \(P_{high}\) close to 0 are
more vulnerable to p-hits producing upsets. To reduce the SET
pulse-widths at the nodes at which \(P_{high}\) is close to 1(0), the
sizes of the restoring p-MOSFETs(n-MOSFETs) can be
increased. Note that since CMOS is a ratio-less logic, gates
can be sized asymmetrically, i.e., n-MOSFET sizes can be
changed irrespective of the corresponding p-MOSFET sizes.
Doing so skews the ratio of rise and fall times, but transition
times are important considerations for critical paths only [3].
As shown in Fig. 2, since such nodes are very few, the
designer can achieve significant SET reduction even by
resizing any one of the p-MOS or n-MOS arrays if the delay is
not an important concern for that logic path.

![Fig. 2. Number of gates hardened by \(P_{high}\) and FM
values (for above three circuits and others) is very low.](image)

<table>
<thead>
<tr>
<th>Node</th>
<th>(P_{high})</th>
<th>Failure Metric</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>0.50</td>
<td>---</td>
</tr>
<tr>
<td>B</td>
<td>0.50</td>
<td>---</td>
</tr>
<tr>
<td>C</td>
<td>0.50</td>
<td>---</td>
</tr>
<tr>
<td>D</td>
<td>0.25</td>
<td>0.56</td>
</tr>
<tr>
<td>E</td>
<td>0.25</td>
<td>0.56</td>
</tr>
<tr>
<td>F</td>
<td>0.48</td>
<td>0.75</td>
</tr>
<tr>
<td>G</td>
<td>0.50</td>
<td>0.26</td>
</tr>
<tr>
<td>H</td>
<td>0.25</td>
<td>0.52</td>
</tr>
<tr>
<td>Z</td>
<td>0.50</td>
<td>1</td>
</tr>
</tbody>
</table>

In case of logical masking, a transient at any node in a
circuit can propagate to the outputs only if the gates between
the node and the output allow the transient to propagate. In
other words the probability that the transient propagates
through to the output is given as the product of the
probabilities of all other inputs of gates lying on the path being
at their enabling values. The \(P_{high}\) numbers for each gate can
then be used to calculate the logical masking ability of
individual gates. For AND, NAND, and XNOR gates, this
enabling value for inputs is 1, whereas for OR, NOR, and
XOR gates, this value is 0. \(P_{high}\) and \((1 - P_{high})\) therefore, give
the probability of that input being at logic 1 and logic 0
respectively. We have defined the probability of a signal
propagating from a node to the output for each gate as the
Failure Metric (FM).
Failure Metric = \[ \sum_{i=1}^{n} \left( \prod_{j=1}^{m} \prod_{k=1}^{l} P_{E_k} \right) \]  

where \( P_{E_k} \) is the enabling value probability for input \( k \) of each gate \( j \), not lying on the path \( i \) from input to output.

Consider a transient at the output of gate G1 to output Z of the circuit in Fig. 1. The failure metric for E is:

\[ \text{FM}(E) = (1-P(D))(1-P(H)) \]  

The inverter does not contribute to logical masking. The failure metric for each node is included in Column 3 of Table 1. The outputs are fully sensitized to transients and have \( \text{FM} = 1 \). Higher values for \( \text{FM} \) correspond to a greater probability of transients at those nodes propagating to the output. Hence the gates corresponding to these nodes must be hardened to reduce the possibility of SETs at such nodes from propagating to the outputs. The \( \text{FM} \) numbers agree with intuition that gates closer to the outputs should have higher values of \( \text{FM} \). In fact a large number of nodes with \( P_{\text{high}} \) close to 1 and 0 also appear on the list of nodes with higher \( \text{FM} \) values. Thus an approach to harden these nodes only, may also be adopted since they represent a sizable proportion of the most vulnerable nodes.

### III. ERROR RATE ESTIMATION

We have defined an Error Metric (EM), which is a useful indicator of the reduction in the circuit SER. A SPICE level analysis of the synthesized ISCAS-85 benchmark circuits was carried out and with knowledge of the commercially available 45-nm Oklahoma State University(OSU) standard cell libraries, the pertinent gates were resized.

The LETs of most particles in space do not exceed 15 Mev-cm²/mg[3]. For a charge collection depth of ~ 1um for the libraries used, this equates to a maximum charge deposition of 150 fC. Charge deposition from 5 fC to 250 fC was simulated using a double exponential current pulse at the nodes that were hardened[13]. Pulse-widths in the range of 15 ps to 220 ps were observed for the unhardened devices and about a factor of 2X and 3X less for devices whose widths were doubled and tripled, respectively. Fig. 4 shows the simulations for charge deposition versus transient pulse-width for a NAND gate. Charge deposition was incremented in small steps and errors reported at the output if the transient amplitude exceeded \( V_{dd}/2 \) and was at least as wide as the setup and hold time for the flip-flops. The results of the EM reduction were observed by considering charge deposition on hardened nodes. The worst case SER of a combinational circuit can be given by

\[ \varphi \left( \sum_{i=1}^{n} A_i \sum_{k=dq}^{Q} dq_k T_{\text{seu}_k/ T_{\text{clk}}} P_{\text{prop}} + \right) \]

Start: Describe circuit in Structural Verilog/VHDL. 
compute \( P_{\text{high}} \), Failure Metric(FM), gate to output delays. 
rank nodes based on both \( P_{\text{high}} \) and FM values. 
resize selected nodes based on \( P_{\text{high}} \) and FM values. 
for (delay > delay constraint) 
\{ remove least vulnerable nodes on maximum delay paths by FM values 
re-compute delay \}
for (area > area constraint) 
\{ remove least vulnerable nodes by FM values 
re-compute area \}
end
where \( \phi \) is the flux particles. \( A_{i(j)} \) is the probability of node \( i(j) \) being struck and collecting charge \( dq_k \) to produce a transient of width \( T_{seu} \). \( Q \) is the maximum charge deposition obtained from SPICE. \( T_{clk} \) is the clock period. \( P_{prop} \) is the probability that the transient is not logically masked by the other gates. \( n \) and \( m \) are numbers of hardened and unhardened nodes respectively.

The most vulnerable nodes in the circuit play a dominant role in determining the SER of the circuit, while transients at the rest have a higher probability of being masked [5]. From Equation 6, this improvement is mainly seen in the first factor for the hardened circuit. Although the probability of being hit is higher for the hardened nodes, the shorter SET pulse-widths correspond to lower latching probability. An analysis of the improvement to be gained by hardening the most vulnerable nodes selectively has been reported as the EM reduction in Column 6 of Table 2.

IV. TEMPORAL MASKING

In order to mitigate propagation of SETs to the output, guard gates have proven effective at reducing the number of SETs that can be latched by storage elements [6, 7]. The representational diagram in Fig. 5 shows the variable delay circuit used to trade-off the number of SETs propagating to the output with the overall delay requirements of the circuit. Since the maximum observed pulse-widths at output were 220 ps, 12 inverters each having a delay of 18 ps were chosen to achieve complete elimination of SETs. Delays of 54ps, 90ps and 144ps could be chosen by the designer to achieve a tradeoff between speed and SET reduction. The area overhead for the variable delay circuit does not exceed 3% for most of the circuits analyzed. To satisfy tight timing constraints, the delay can be set to zero resulting in no elimination of the transients that appear at the Guard Gate inputs. The delay overhead in Column 4 of Table 2 includes the delay introduced by Guard Gates.

![Variable Delay Guard Gate circuit.](image)

Table 2: Percentage overheads in terms of area, power, and delay and Error Metric reduction of the 2X hardened circuits.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Area (%)</th>
<th>Power (%)</th>
<th>Delay (with GG)</th>
<th>Delay Reduction (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C432</td>
<td>12</td>
<td>04</td>
<td>24</td>
<td>33</td>
</tr>
<tr>
<td>C499</td>
<td>11</td>
<td>03</td>
<td>18</td>
<td>23</td>
</tr>
<tr>
<td>C880</td>
<td>07</td>
<td>07</td>
<td>27</td>
<td>31</td>
</tr>
<tr>
<td>C1908</td>
<td>16</td>
<td>09</td>
<td>33</td>
<td>46</td>
</tr>
<tr>
<td>C2670</td>
<td>08</td>
<td>08</td>
<td>35</td>
<td>30</td>
</tr>
<tr>
<td>C3540</td>
<td>12</td>
<td>09</td>
<td>21</td>
<td>24</td>
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<tr>
<td>C5315</td>
<td>09</td>
<td>11</td>
<td>39</td>
<td>37</td>
</tr>
<tr>
<td>C6288</td>
<td>12</td>
<td>08</td>
<td>25</td>
<td>47</td>
</tr>
<tr>
<td>C7552</td>
<td>13</td>
<td>10</td>
<td>32</td>
<td>21</td>
</tr>
</tbody>
</table>

V. CONCLUSION

A computationally efficient algorithm has been proposed to estimate the effects of logical masking. It can be used as a low-cost estimate of the reduction in SET pulse-widths to be gained from selectively increasing the sizes of certain gates. Variable-delay guard gates can be used to further reduce the number of SETs that can be latched and hence achieve a lower SER at the cost of slower speeds.

REFERENCES